Hybrid Electromagnetic Simulation for 3D package Integration

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3D Integration Using Through-Silicon-Via

International Roadmap for Semiconductors (ITRS): http://www.itrs.net/

Courteous of Prof. Andreas Cangellaris
ITRS – Modeling & Simulation: Difficult Challenges

Circuit element and system modeling for high frequency (up to 160 GHz) applications

- **Supporting heterogeneous integration** (SoC+SiP) by enhancing CAD tools to simulate mutual interactions of building blocks, interconnects, dies and package:
  - Possibly consisting of different technologies
  - Covering and combining different modeling and simulation levels as well as different simulation domains

- **Computer-efficient inclusion of variability** – including its statistics (including correlations) before process freeze – into circuit modeling, treating local and global variations consistently
Modelling of Multilayered IC Packages
Semi-analytical Method
IEEC Method – Modal Decomposition

Decouple the original complex three-dimensional problem into several simple two-dimensional, one-dimensional, and zero-dimensional sub-problems;

Extract the equivalent circuits of each sub-problem through specially selected analytical and numerical methods;

Recombine the obtained equivalent circuits together.

Integral Equation Equivalent Circuit (IEEC) Method

- Advantages:
  1. Make a full use of the geometric features of the electronic package;
  2. Give a fast simulation and still keep a good accuracy;
  3. Equivalent circuits model gives a more comprehensive solution for industrial engineers than pure electromagnetic field solvers.

Courteous of X. C. Wei
2D Integral Equation Solution for Power and Ground Planes

Power and ground planes are metals with a high conductivity.

\[ E_x = E_y = H_z = 0 \]

Distance between power and ground planes is much smaller than wavelength of interest.

\[ \frac{\partial E}{\partial z} = 0 \]

\( E \) and \( H \) field are uniform along \( z \).

The power and ground planes can be taken as a 2D transverse magnetic (TM) problem.

_Courteous of X. C. Wei_
Step 1: Define Voltage and Current between Each Pair of Planes

Vertical voltage \( V = -d \times E_z \) with \( d \) being the thickness of the substrate.

Horizontal currents

\[
\hat{J} = -\hat{z} \times \hat{H} \quad \text{on the up plane} \\
\hat{J} = \hat{z} \times \hat{H} \quad \text{on the down plane}
\]
Step 2: Create Integral Equation along the Periphery of Power-Ground Planes and the Anti-pads

\[ V(r) = \frac{k}{2j} \oint_C \left[ \hat{R} \cdot \hat{n}' H_1^{(2)}(kR)V(r') + j\eta d H_0^{(2)}(kR)J_n(r') \right] dl' \]

C: Periphery of power-ground planes and anti-pads.

This integral equation creates the relationship between the defined voltages and currents.

$I_{\text{trace}}$ is the current along the signal trace.

$J_a$ is its return current. $J_a$ starts from the top plane, passes through the distributed $RLCG$ (resistance, inductance, capacitance, and conductance) of the power-ground pair, and arrives at the bottom plane.

Via’s parasitic $L&C$ is not included in this Integral Equation yet. Via’s equivalent circuit will be extracted later.
Step 3: Discretize the Integral Equation

$(V, J_n)$ are expanded by using unit pulse functions defined along periphery and each antipad.

$$V_a (r) = \sum_{i=1}^{N_a} V_{a,i} P_{a,i} (r)$$

$$V_p (r) = \sum_{i=1}^{N_p} V_{p,i} P_{p,i} (r)$$

$$J_a (r) = \sum_{i=1}^{N_a} I_{a,i} P_{a,i} (r) / w_{a,i}$$

$$J_p (r) = \sum_{i=1}^{N_p} I_{p,i} P_{p,i} (r) / w_{p,i}$$

$$P_{p/a,i} (r) = \begin{cases} 1, & r \in w_{p/a,i} \\ 0, & r \notin w_{p/a,i} \end{cases}$$

Subscript $p$ and $a$ denote the periphery and antipad respectively. $w_{p/a,i}$ represents the $i$th straight segment/circle.
Each Power-Ground Plane is equivalent to a N-port network
Step 3: Discretize the Integral Equation

Matching both sides of integral equation with $r$ at the center of each peripheral segment and antipad.

$$
\begin{bmatrix}
U_{pp} & U_{pa} \\
U_{ap} & U_{aa}
\end{bmatrix}
\begin{bmatrix}
V_p \\
V_a
\end{bmatrix}
=
\begin{bmatrix}
H_{pp} & H_{pa} \\
H_{ap} & H_{aa}
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_a
\end{bmatrix}
$$

Moment Matrix
Step 4: Matrix Reduction

A perfect magnetic wall is assumed along the periphery due to the thin layer. Therefore, $[I_p]=0$.

$[Z^a] \cdot [I_a] = [V_a]$

Impedance matrix of the ground network

$[Z^a] = ([U^{aa}] - [U^{ap}] \cdot [U^{pp}]^{-1} \cdot [U^{pa}])^{-1} ([H^{aa}] - [U^{ap}] \cdot [U^{pp}]^{-1} \cdot [H^{pa}])$

The elements in $[Z^a]$ represent the self and mutual ground impedances for the signal traces passing through the same power-ground pair.
Formulation- 2D Integral Equation Solution for Power-Ground Planes

Validation of the Ground Network

Test Structure (unit: mm)

Computing Time
Full-Wave: 7Min.
Proposed IEEC: 10s

Full-Wave De-embedding Extraction Methods for Multi Through-Hole Vias (THVs)

- Full-wave extraction method can solve multi THVs with arbitrary shapes and medium, and provide the accurate frequency-dependent equivalent circuit.
- It is also efficient since the computational domain only includes the small THVs region, no need to consider the whole power distribution network.
- Parasitic capacitance is defined between the THVs and the power-ground planes, so certain part of the power-ground planes must be included during the extraction. However, the planes also introduce unwanted parallel plate mode’s effect.
- An easy de-embedding method is proposed to remove the unwanted parallel plate mode’s effect.
IEEC Method – Modal Decomposition

Decouple the original complex three-dimensional problem into several simple two-dimensional, one-dimensional, and zero-dimensional sub-problems;

Extract the equivalent circuits of each sub-problem through specially selected analytical and numerical methods;

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From Maxwell Equations to Equivalent Circuits

Power-Ground Planes (Two-dimensional)

Standing wave

Signal Traces (One-dimensional)

Propagation wave

Transmission Lines

Lumped Circuits

Vias Edges & Gaps

Discontinuities (Zero-dimensional)

Extraction of Equivalent Circuit of Discontinuities

- Provide frequency dependent equivalent capacitance and inductance
- Application is limited to vias with regular shapes

\[
L = \frac{\mu}{2\pi} \left[ h_1 \ln \left( \frac{0.5413 h_1}{a} \right) + h_2 \ln \left( \frac{0.5413 h_2}{a} \right) \right]
\]

\[
k_n = \sqrt{\left( \frac{n\pi}{2h_{1/2}} \right)^2 - 1} / \lambda_g^2
\]

\[
C_{1/2} = \frac{4\pi \varepsilon}{[h_{1/2} \ln (b/a)]} \sum_{n=1,3,5,...}^{\infty} \left[ 1 - K_0 \left( k_n b \right) / K_0 \left( k_n a \right) \right] / k_n^2
\]

Extraction of Equivalent Circuit of Discontinuities

Extraction of Equivalent Circuit of Vias--Deembedding Method

Vias+PGP structure

Equivalent Circuit of Vias+PGP

Cascade of $ABCD$ matrices

$$[T]_{vias+PGP} = [T]_{vias} \times [T]_{PGP} \times [T]_{vias}$$

Recombination: Power-Ground Planes + Signal Traces + Discontinuities
Numerical Examples

Two Coupled Signal Traces Passing through one Power-Ground Planes Pair

Structure (unit: mm)

Side view

Top view

Computing Time
Full-Wave HFSS: 20Min.
Proposed IEEC: 15s

|S_{11}|

|S_{31}|

|S_{41}|

Frequency (GHz)

Frequency (GHz)
Signal Trace Passing through Four-Layered PGPs

Structure (unit: mm)

Side view

Top view

Computing Time
HFSS: 1Hour
IEEC: 12s

Equivalent circuits of the structure.
Numerical Examples

Four Coupled Signal Traces + Three Power-Ground Planes Pairs + Power&Ground Vias

Structure (unit: mm)

Top view

Port 1
Port 4
(20,41.5)
0.5
Coupled SL (60,41.5)
Port 2&3
Port 5&6
Coupled MS1 (20,40)
Power Pin (20,25)
(35,25) Hole 10
Ground Pin (50,25)
(55,10) Coupled MS3
Port 7
Port 9
0.5
Power Plane 1
PGP1
Power Plane 2
PGP2
Ground Plane 1
PGP3
Ground Plane 2

Power Pin
Ground Pin
Up Two Traces
Bottom Two Traces

Side view

Port 1 or 4
Port 2 or 5
Port 3 or 6
Port 7 or 9
Port 9 or 10
0.5
IHPC
Numerical Examples

Four Coupled Signal Traces + Three Power-Ground Planes Pairs + Power&Ground Vias

Equivalent Circuits
Numerical Examples

Four Coupled Signal Traces + Three Power-Ground Planes Pairs + Power&Ground Vias

<table>
<thead>
<tr>
<th></th>
<th>Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21</td>
<td>Full-Wave HFSS</td>
</tr>
<tr>
<td>S11</td>
<td>Full-Wave HFSS</td>
</tr>
<tr>
<td>S41</td>
<td>Full-Wave HFSS</td>
</tr>
<tr>
<td>S51</td>
<td>Full-Wave HFSS</td>
</tr>
<tr>
<td>S81</td>
<td>Full-Wave HFSS</td>
</tr>
</tbody>
</table>

Computing Time
HFSS: 4Hour
IEEC: 5Min.
Framework: Integration of Solvers

Pre-Processing

- Geometry Model
  - User Input
  - Import CAD (PKG design)

- Translator
  - Data for Engine
  - Meshing

Engine/Solver

- Via-circuit model
- Plate Pair Model (Zpp)
- PI Analysis
  - Multilayer
  - Decoupling Capacitor
- SI Analysis (Trace)

Post-Processing

Results Visualization

- S/Y/Z
- Eye Pattern
- BER (Bit Error Rate)
- Jitter
- ...
Developed EDA Simulation Software Tool

EDA: Electronic Design Automation, an Industry Design Tool
Import a Benchmark Package from IBM®

Having 11,000+ vias inside the electronic package

Identifying a signal trace or a via in the layout
Test Circuit for Signal Integrity Analysis

PRBS: pseudorandom binary sequence source
Integrated Circuits (IC) Packaging

TX (Transceiver) → Comm. Path (channel) → RX (Receiver)

MOS Transistors
Moore’s Law
Scaling of Transistor
shorter gate length (smaller gate-delay)

Interconnect
No Law
high signal speed
shorter line (smaller line-delay)

TSV


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Electrical Modeling for SI/PI/EMI

- Full wave simulation
- Or equivalent circuit approaches
Questions: 1) Is TSV a big deal? 2) How much benefit - quantify? 3) model for design & analysis

TSV = 1) Coated metal wire; 2) MOS Cap; 3) thermal effect

--- Electrical modeling & evaluation ---

What effects shall be considered?

- Skin effect
- Loss effect of silicon
- Proximity effect
- MOS capacitor effect
- Thermal impact

References:
# Ideal MOS Cap effect (2009), Prof. Swaminathan’s group at GIT
# MOS Cap effect with oxide charge (2010) Group at IMEC
Equivalent Circuits for TSVs (With Closed-Form Formulae)

Tree vs. Forest Approach

TSVs in ground-signal (GS) Configuration

- Skin effect
- Proximity effect
- Loss effect of silicon

Can we derive an equivalent circuit model – faster rigorous model & accurate & the three effects?
Equivalent Circuits for TSVs (With Closed-Form Formulae)

TSVs in ground-signal (GS) Configuration

Pi-type physical model

[Ref.] Prof. Kim’s group at KAIST, 2006, ESTC
Equivalent Circuits for TSVs (Validation)

Compare results by this work and HFSS simulation.
Through-Silicon Via (TSV)-MOS Capacitor Effect

Charges in an $n$-type MOS structure with $p$-type substrate under different modes of operation.
Through-Silicon Via (TSV)-MOS Capacitor Effect

Poisson’s equation

\[
\frac{1}{r} \frac{d}{dr} \left( r \frac{d \phi(r)}{dr} \right) = \frac{q}{\varepsilon_{si}} \frac{N_a}{\varepsilon_{oi}}
\]

\[
C_g = \left( \frac{1}{C_{ox}} + \frac{1}{C_d} \right)^{-1}
\]

\[V_{FB} < V_{tsv} < V_T\]
Reflection and transmission coefficients of TSVs considering MOS Capacitor effect
Through-Silicon Via (TSV)-Thermal Equivalent Circuit for Electrical Evaluation

Thermal Integrity of TSV & 3D IC

- 15 °C increase in Temperature:
  - delay up by 10-15%
  - resistance up by 10%

- Reliability issue

Temperature profile of a TSV due to

- self (or Joule) heating,
- substrate heating
- heat conduction from neighboring TSVs & interconnects

![Thermal Equivalent Circuit](image)

- thermal equivalent circuit
- electrical equivalent circuit

SPICE

**a thermal equivalent circuit model**
Through-Silicon Via (TSV)-Summary of Multi-physics Modeling with Circuit Approach

(3 Aspects within 1 Framework)

High Frequency - Maxwell Eqs.

Closed-form formulae for RLCG –
- rigorous & accurate -

Low Frequency – Semicon. Physics
(Poisson/ Quantum?)
MOS cap effect - a simple but unified treatment

TSV

Equivalent circuits

SI/PI/EMI/TI

Thermal Impact -
Heat Diffusion Eq.
Thermal equivalent circuits
Polymer Cavity TSV Structure

(a) Polymer Cavity TSV details

(b) Multiple TSV in Polymer Cavity

(c) Polymer cavity in Si substrate
Test Vehicle

a) Model used for simulation

- Polymer Substrate
- GSG TSV with probe pad
- CPW Transmission line

b) Fabricated test vehicle – focus on the top layer

- GSG TSVs
- Polymer Cavity
- GSG probe pads

b) Fabricated test vehicle – focus on the bottom layer

- IHPC
Measurement Results

GSG wafer probe with 100µm pitch

Test vehicle

Styrofoam

Chuck

Via-line-via loss up to 110GHz ~1dB

Insertion Loss (dB)

Return Loss (dB)

freq. GHz

freq. GHz

Measured

Simulated
Concluding Remarks

An novel Integral Equation Equivalent Circuit method is developed and validated.

The advantages of the proposed method are:

- Decouple the complex three-dimensional power distribution network problem into several simple two&one-dimensional problems. Greatly reduce the computing time and still keep a good accuracy.

- Extract the equivalent circuit model from the field problem. Can be easily substituted into any available circuit simulators.