3D Enablement Center

(from Larry Smith, SEMATECH)
3D Enablement Center

- Program announced December 2010 by SEMATECH, SIA, and SRC
  - Designed to meet diverse needs of SIA members: high performance, mobile, analog, mixed signal, MEMS, fabless, fablite, IDMs
  - Address gaps identified in SEMATECH industry-wide survey
- Mission:
  - Enable industry-wide ecosystem readiness for cost effective TSV-based 3D stacked IC solutions
- Members include:
  - Enablement Center: ASE, Altera, ADI, LSI, ON Semi, and Qualcomm
  - SEMATECH: CNSE, GLOBALFOUNDRIES, Hewlett Packard, Hynix, IBM, Intel, Samsung, and UMC

- Phase 1 Activities
  - Technology and specifications supporting SEMI Standards
  - Standards landscape (“dashboard”)
  - Inspection/metrology: TSV and bond voids, wafer thickness and warpage
  - Microbumping and bonding specifications
  - University research managed by SRC
- Initial focus in Phase 1 is on Wide IO DRAM for mobile applications
  - Provide clarity to help identify gaps in standards, specifications, technologies
  - But will also explore high performance computing, analog/MEMS, etc…
- Future phases (separately funded) of this program may include:
  - Pathfinding
  - EDA tools
  - Test vehicles
SEMATECH survey: gaps in via-mid ecosystem

**Highest priorities** for heterogeneous stacking (e.g., wide IO DRAM):

**Gaps in Standards and Specifications**
- EDA exchange formats
  - Partitioning and floorplanning; Logic verification; Power/Signal integrity analysis; Thermal analysis flow; Stress analysis flow; Physical verification; Timing analysis
- Reliability
  - Reliability test methods
- Test
  - DFT test access architecture
- Inspection/metrology
  - TSV voids, defect mapping, microbump inspection and coplanarity
- Chip interface
  - Stackable memory pin assignment; Stackable memory physical pinout
- TSV
  - Keep out area, fill materials, dimensions
- Thin wafer handling
  - Universal thin wafer carrier

**Technology Development and Cost Reduction**
- Reliability
  - Criteria; Test methods; ESD
- Temporary bond/debond cost reduction
  - Materials and release mechanisms cost reduction; Equipment cost reduction
- TSV
  - Keep out distance/area
- Microbumping and bonding
  - Pad metallurgy and layer thickness; Bump metallurgy
- Inspection/metrology
  - Microbump inspection and coplanarity; TSV voids; BWP voids
- Test
  - Probing microbumps cost reduction
Wide IO DRAM

Initial Target Vehicle
Cross-section Slice (not to scale)

- Tier 2
  - Thickness ~ 260 μm
  - Active Face Down

- Underfill
  - Gap ~ 20 μm

- μ-Bump
  - Pitch ~ 25-50 μm

- BackSide Metal
  - Pitch ~ 5-25 μm

- Tier 1
  - Thickness ~ 50 μm
  - Active Face Down

- Underfill
  - Gap ~ 80 μm

- Flip Chip Bump
  - Size ~ <100 μm
  - Pitch ~ 100-200 μm

- Package Substrate
  - Thickness ~ 180 μm

- TSV
  - Size ~ 5-10 μm
  - Pitch ~ 10-50 μm

- BGA Bump
  - Pitch ~ 0.65 mm
  - Height ~ 300 μm
SEMATECH 3D Enablement Center

University Reliability Research

Standards & Metrology Working Group

Design Exchange Format Working Group

SEMI

Manufacturing Standards

Si2

Design Standards

GSA 3D SiG
Reliability Activity Update
June 13th, 2011
Reliability Taxonomy Development Goal:

Investigate reliability of 3D heterogeneous circuits and classify the different anticipated failure mechanisms, especially those unique to TSV-based 3D stacked IC assemblies.
First Steps:

1. Organize a team of Experts from Academia from several different and synergistic disciplines

2. Create an RFP and solicit short term research proposals
   - The initial output from the program should be a compendium of potential failure mechanisms
   - The program longer term should validate and recommend test structures as well as develop calibrated and predictive models

3. Select and fund proposals for investigating fundamental causes of prioritized failure mechanisms
Reliability Workshops, March 17th:

• Design for Reliability Workshop – Stress Management for 3D ICs Using Through Silicon Vias
  • Purpose: Work towards an understanding of the mechanical stress-driven failure mechanisms, associated test vehicles, and characterization and modeling methodologies which pertain to the via-middle through-silicon-via (TSV) 3D stacking technologies

• 3D EC Reliability University Research Project Kick-off
  • Purpose: Develop a table of prioritized stress-related failure mechanisms, test structures, test regimes, and modeling approaches
  • Begin draft of RFP for solicitation of short term University research proposals
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3. Select and fund proposals for investigating fundamental causes of prioritized failure mechanisms
Status:

• 12 proposals received and are in evaluation

• Final selection expected by June 30th, with task starts by Aug. 1st
Design Exchange Activity Update
June 13th, 2011
3D Design Exchange Format Development Goal:

Design and build a set of open exchange formats to support the 3D design tool interface standardization activities, enabling designs from different vendors to cohabitate within a given architecture.
First Steps:

1. Organize a team of Experts from Academia to define a prioritized list of required 3D Design Exchange Formats
   - What is the complete set of design information about a Wide I/O Memory to design the Logic die underneath it with minimum risk?

2. Develop a set of specific Exchange Format drafts to be delivered to the Si2 for their feedback, refinement, and ultimate adoption

3. Provide feedback to Si2 on the technical merits/issues of their developed standards proposals

4. Create a proposal for longer range 3D design tool research work
<table>
<thead>
<tr>
<th>Technical area</th>
<th>Driver</th>
<th>Stds Body</th>
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<tbody>
<tr>
<td>PF Exchange Formats</td>
<td>3D EC</td>
<td>Partitioning info, floorplanning info</td>
</tr>
<tr>
<td>Stress Exchange Formats</td>
<td>IMEC ?</td>
<td>I/P for stress sim + O/P Stress Map</td>
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<tr>
<td><strong>Thermal Exchange Formats</strong></td>
<td>3D EC</td>
<td>I/P power map + O/P Temp map for timing</td>
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<td><strong>Power Delivery Network Exchange Format</strong></td>
<td>3D EC</td>
<td>Reduced order compact power model</td>
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<td>Signal Integrity Exchange Format</td>
<td>3D EC</td>
<td>Equivalent of IBIS-like mod for 3D</td>
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<tr>
<td>DFT Exchange Formats</td>
<td>IMEC</td>
<td>To enable Scan/JTAG across tiers</td>
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(from Riko Radojcic, Qualcomm)
Next Steps:

1. Organize a team of Experts from Academia to define a prioritized list of required 3D Design Exchange Formats
   - What is the complete set of design information about a Wide I/O Memory to design the Logic die underneath it with minimum risk?

2. Develop a set of specific Exchange Format drafts to be delivered to the SI2 for their feedback, refinement, and ultimate adoption

3. Create a proposal for longer range 3D design tool research work

4. Provide on-going feedback to SI2 on the technical merits/issues of their developed standards proposals
Status:

• PI’s to self-organize in to small teams, each to deliver initial 2-3 page draft outline for Thermal and/or PDN design exchange formats by June 24th
  • Also expected in these deliverables is a brief 1-page proposal for longer range, next-step work

• Drafts will be reviewed and combined in on-line workshop to be scheduled by June 30th; output to be delivered to SI2 for feedback