Thermo-Mechanical Reliability Challenges of 3D Interconnects

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SRC Project Review, June 14, 2010
3D Integration

A wide variety in 3D design and application
Thermomechanical Reliability Issues?

Philip Garrou, 2008

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3D Process Options: Front Side TSV

Via last TSV
Fraunhofer

Via middle TSV
Freescale
R. Jones et al. IEEE CPMT 2009

Processing and geometry can lead to distinct stresses and failure modes for TSV structures

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3D Process Options: Backside TSV

- **Carrier wafer**
- **Via etched from the backside to the Back of the peripheral pads**
- **Redistribution on backside of wafer**

Typical wafer thickness 100-150 um
Typical TSV dia 50-75 um
Conformal Cu (5-10 um thick) not full plug
Filled with CTE matched material

Vias last from the backside

*Philip Garrou, 2009*
TSV Mechanical Reliability

➢ Stress around TSVs:
  • *Keep-away zone* for FEOL
  • Cracking of silicon

➢ Stress at the interfaces:
  • Debonding, TSV pop-up

➢ Stress inside TSVs:
  • Plastic deformation
  • Stress-induced voiding
  • Stress migration

❖ Sources of stress:
  • Process-induced stress
  • Thermal stress – BEOL process
  • Packaging induced stress

TSV stress and reliability depends on both materials processing and structural design.

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Outline

• Process-induced stresses in 3D structures
• Stress analysis of TSV structures
  2D and 3D analytical solutions
  Finite element analysis
• Fracture of TSV structures
  Interfacial delamination (TSV pop-up)
  Matrix cracking – r crack and c crack
• Effect of TSV metallization: Al, Cu, Ni, W
  ERR for TSV with nail head structure
• Adhesion and fracture energies for Cu interfaces
Stress Analysis of TSV Structures

- **Process induced stresses**

- **Analytical solutions**
  - 2D approximation
  - Near-surface stress distribution by method of superposition

- **Finite element analysis**
  - Effect of liners/barrier layers
  - Effect of wafer thickness
  - Effect of elastic mismatch
  - Effect of nail head

*FEA Model*
3D Integration: Via Middle Process

TSV materials:
- Conductors: Cu, W
- Insulators: TEOS, polymers
- Barrier/adhesion: TiN, TaN

Geometric aspects:
- High aspect ratio
- Thin Si wafer (~10-300μm)
- Diameter (~1-50μm)
- Pitch (~3-100μm)

Step A
Step B
Step C
Step D
Step E

R. Jones et al. IEEE CPMT 2009

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Process Induced Stress Simulation

- TEOS/barrier layer deposition at 400~430°C
- Cu electroplating @ 30°C, Annealing @ 200°C
- Cooling down to 30°C, Cu CMP
- Capping layer deposition at 150°C
- CVD of TEOS @ 400°C
- Cooling down to 25°C

Critical steps for interfacial delamination and silicon cracking.

TSV diameter: ~2 μm

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Process Induced Stress Simulation

- CVD of TEOS @ 400°C
- Cooling down to 25°C

TSV diameter: 2μm

- Shear stress and tensile normal stress at TSV corners can induce interfacial delamination

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Thermal Stress: 2D Approximate Solution

Thermal Strain:

\[ \varepsilon_T = (\alpha_{Cu} - \alpha_{Si})\Delta T \]

Uniform thermal stress in Cu via (triaxial):

\[ \sigma_r = \sigma_\theta = \frac{-E\varepsilon_T}{2(1-\nu)}, \quad \sigma_z = \frac{-E\varepsilon_T}{1-\nu} \]

Stress distribution in Si (biaxial):

\[ \sigma_r = -\sigma_\theta = \frac{-E\varepsilon_T a^2}{2(1-\nu) r^2}, \quad \sigma_z = 0 \]

- The magnitude of the stresses in the via is independent of the via size.
- The stresses in Si decay with the distance \( r \), with the decay length proportional to the via size \( a \).
2D Stress Field of Single Via

- Cooling from the reference temperature (\( \Delta T = -175^\circ C \)) leads to tensile stresses in the via. Zero stress reference at 400\(^\circ\)C.
- Around the via, the stress is tensile in the radial direction and compressive in the circumferential direction, both concentrated near the via.
Proximity Effect on Keep-away Zone

- Proximity of TSVs increases the area with high thermal stress and affect the keep-away zone.

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For TSV with high aspect-ratio, the stress field away from the surfaces can be obtained from a 2-D plane-strain solution (Problem A).

The stress field near surface is 3-D, which can be determined by superimposing an opposite surface loading (Problem B) onto the 2-D field (Problem A) to satisfy the boundary conditions at the surface.
Stresses near Wafer Surface

- **σₗ** Stress Contour
- **σᵣᵢ** Stress Contour

Positive opening stress along Cu/Si interface

Concentration of the shear stress at the surface/interface junction
FEA: Effect of Wafer Thickness

At the Cu/Si interface, the opening stress ($\sigma_r$) decreases but the shear stress ($\sigma_{rz}$) increases as the aspect ratio $H/D$ decreases.
Effect of Liner Interlayer

\[ \sigma_r \]
opening stress

\[ \sigma_{rz} \]
shear stress

Without liner  
With liner

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Potential Fracture Modes of TSVs

R-crack may grow in Si during heating ($\Delta T > 0$) when the circumferential stress is tensile ($\sigma_\theta > 0$).

C-crack may grow in Si during cooling ($\Delta T < 0$) when the radial stress is tensile ($\sigma_r > 0$).

Interfacial crack can grow during both heating and cooling, leading to pop-up of TSV.
Concepts of Fracture Mechanics

- **Energy release rate** (ERR or $G$): thermodynamic driving force for crack growth, the elastic strain energy released per unit area of the crack; calculated by FEA or other methods.

- **Fracture toughness** ($\Gamma$): material resistance against cracking, an intrinsic property of the material or interface; measured by experiments.

  $$G > or < \Gamma$$

- **Cohesive zone modeling**: use a nonlinear traction-separation relationship to describe the interactions across the interface, including crack nucleation and growth.
TSV Interfacial Delamination

- Heating cycle ($\Delta T > 0$): Interfacial crack driven by shear stress ($\sigma_{rz}$); Mode II fracture

- Cooling cycle ($\Delta T < 0$): Crack driven by both shear stress ($\sigma_{rz}$) and radial stress ($\sigma_r > 0$); mixed mode fracture (Mode I + Mode II)
Energy Release Rate (ERR)

\[ \Delta T = -250 \text{ K} \]

\[ \Delta T < 0 : \text{Mode I+II} \]

\[ G_{SS}^{cooling} \approx \frac{E(\Delta \alpha \Delta T)^2 D_f}{4(1-\nu)} \]

\[ \Delta T > 0: \text{Mode II} \]

\[ G_{SS}^{heating} \approx \frac{1+\nu}{8(1-\nu)} E(\Delta \alpha \Delta T)^2 D_f \]

- The steady-state ERR sets an upper bound for the crack driving force, which may be used for conservative design.

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Crack Driving Force ERR for TSV Delamination:

Assumption:
1. Linear elasticity
2. No friction, no elastic mismatch
3. Infinite long fiber, long crack length

Steady-State Solution of Energy Release Rate, $G_{ss}$:

$$G_{ss} = \frac{\Delta U}{2\pi a} = \frac{E(\Delta \alpha \Delta T)^2}{2(1 - \nu)} a$$

$G_{ss}$ increases with thermal load and TSV diameter
ERR for TSV Delamination: Annular TSV

Assumption:
1. Linear elasticity
2. No friction, no elastic mismatch
3. Infinite long fiber, long crack length

Steady-State Solution for Annular TSV:

\[ G_{SS} = \frac{E(\Delta \alpha \Delta T)^2 r_2}{2(1-v)} \left(1 - \mu^2\right) \]
ERR for TSV Delamination: Fixed Annular Thickness

From A to E: $r_2$ increases 20x while $G_{SS}$ increases only ~2x. ERR can be minimized by reducing annular thickness.
ERR in Nail-Head Structure (Vertical Crack under Cooling)

• "Nail-Head" pop-up: First vertical delamination during cooling followed by horizontal cracking during heating.

Steady-State Solution of Energy Release Rate, $G_{SS}$:

$$G_{SS} = \frac{E(1 + \nu)(\Delta \alpha \Delta T)^2}{4(1 - \nu)} a$$

Vertical axial symmetric crack

$D_f = 20\mu m$, $\Delta T = -250^\circ C$

**Figure:** ERR for vertical crack

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TSV with Nail Head

- Shear stress at both interfaces
- Opening stress at the NH/Si interface (heating)

\[ D_f = 6 \mu\text{m} \]
\[ \Delta T = 400 \text{ K} \]
Cu TSV/NH subjected to heating up to +400K
Cohesive interface elements are used to for both via/Si and NH/Si interfaces
Effect of TSV Metals

- The effect of thermal mismatch dominates the effect of elastic mismatch.

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Annular TSV

Diameter ratio: \[ \eta = \frac{D_i}{D_f} \]

Steady-State ERR for interfacial delamination:

\[
G_{SS} = \frac{E_{Si} (\Delta \alpha \Delta T)^2 D_f}{4} f\left(\eta, \frac{E_{TSV}}{E_{Si}}, \nu_{TSV}, \nu_{Si}\right) \approx \frac{E (\Delta \alpha \Delta T)^2 D_f}{4(1 - \nu)} \left(1 - \eta^2\right)
\]
Metal Adhesion to SiO₂

\[ \Gamma_O \approx N(H_M + H_O - H_{M-O}) \]

\[ \Gamma_O = \alpha - N(H_{M-O}) \]

Plot of \( G_o \) vs \( H_{M-O} \) should give straight line with slope of \( N \).

<table>
<thead>
<tr>
<th>Metal</th>
<th>( \Delta H_f^a ) (kCal/non-metal atom)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt</td>
<td>-10</td>
</tr>
<tr>
<td>Cu</td>
<td>-39</td>
</tr>
<tr>
<td>W</td>
<td>-70</td>
</tr>
<tr>
<td>Ta</td>
<td>-98</td>
</tr>
</tbody>
</table>

\( \Gamma \) for Si: 5-6 J/m²


Cu has weak adhesion to SiO₂ compared with W and Ta
The Cu/TaN interface can be significantly strengthened with plasticity. Increasing Cu thickness will facilitate yield to improve the fracture energy.

For Cu TSV with TaN barrier and 10 μm dia., the fracture energy increases from 5 J/m² to 40 J/m².

Ni is similar to Cu in its yielding behavior with plasticity to improve interfacial toughness but W is difficult to yield.


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Summary

- Thermal expansion mismatch induces stresses in TSV and surround materials. TSV geometry and material combination can generate complex 3D stress fields that affects the determination of keep-away zone.
- Interfacial delamination of TSV can occur under both heating and cooling while r-crack in Si could occur under heating. In both cases, the crack driving force increases with the TSV diameter and scales with the square of thermal loading.
- The reliability of TSV structure can be improved by optimizing the materials and geometry to reduce the crack driving force.
- Cohesive zone modeling could be useful in the study of crack nucleation and growth, for which experimental measurements of the interfacial properties (toughness and strength) are needed.
Acknowledgement

Discussion with
  Phil Garrou, Microelectronic Consultant, NC
  Michael Lane, Emory and Henry College, VA
  Mike Shapiro, IBM
  Bob Jones, Zhihong Huang, Freescale

Funding Support
  Semiconductor Research Corporation