TSV and Interposer technologies at Allvia
Outline

- Introduction
- TSV Technology
- Silicon Interposers and Embedded Capacitors
- Reliability Summary
- Conclusions
Introduction to Allvia Inc.

- **ALLVIA provides:**
  - Si TSV Interposers with Integrated Capacitors
  - TSV Via Foundry Service for Semiconductor, RF & MEMS industry
  - Support for 3D Integration

- **Intellectual Property**
  - Process, Architecture and Equipment IP (trade secrets and 25+ patents)

- **ALLVIA Facilities:**
  - Sunnyvale: 6,000 sq.ft., clean room in a 20,000 sq.ft. facility
  - Portland, OR: Acquired New Clean room facility for expansion.
    - 60,000 Sq. ft. Clean Room in a 178,000 Sq. ft. facility.

- **ALLVIA partnering with CMOS foundry**
  - Provide CMOS backend multilayer routing integrated with Capacitors and TSV
Through Silicon Via (TSV) Technology: Overview

- We focus on **Two Types of TSV Technologies**
  - Via First → Blind Filled Via → *Front Side TSV*
    - Advantageous for MEMS applications.
  - Via Last → Coated Via → *Backside TSV*
    - Advantageous for processed device wafers.
TSV Technology
Front Side TSV

1. Litho & Via etch
2. Via oxidation
3. Barrier/seed layer dep
4. Via plate w/ Cu
5. CMP front side
6. Front Side Routing + Cap processing
7 A. Thinning, Passivation and Pad Pattern
   OR
7 B. Thinning, Pillar exposure and Oxide Etch
8. Solder bumping
Front Side TSV

Solder Attach
- Pillar Prep
- Solder ball attach

50um dia, 125um Si

Substrate Assembly
65,125Si
Back Side TSV

1. Front Side Protection
2. Wafer Thinning
3. Litho and Via etch from backside
4. Via isolation layer dep. Litho And Oxide Etch
5. Barrier/seed layer dep.
6. Via Cu plate
7. Passivation layer and Litho
8. Bumping
Backside TSV

50um

100um
Silicon Interposer and Embedded Capacitors
Si-BT Flip Chip Interposer

Flip Chip TSV Silicon Interposer

- **TSV**
- *Interconnect layers* on one side or both sides
  - Cu/Pi interconnect layers on one surface (5 um lines/spaces)
  - CMOS backend layers (1um lines and spaces) with Backside TSV
- Built in Capacitor (1500 nF/cm2 +)
- Solder Bump or Cu Pillar on the backside
- Smallest (Chip Size) Interposer for Cost and Reliability

Fine pitch flip chip solder bumps (<150um)

**Cu Spreader / Heat Sink Attach**

**Simple BT or Ceramic substrate**

Flip Chip TSV based Si interposer with routing layers and decoupling capacitors (1500nf/cm2 +)

Under filled flip chip attach
Interposer Test Device

- Interposer Top
- Interposer Bottom
- Interposer on BT substrate
Reliability Summary
Reliability: TSV Filled and Conformal Vias; Interposers

- Thermal Cycling
  - Temp Cycle B (-55C to 125C)
  - Electrical testing: Before and after Thermal Cycling
  - Optical Inspections: Before and after Thermal Cycling
  - Read Outs: 0 Cy., 500 cy., 1000 cy..

- Filled Via Test Wafers
  - 150mm Wafers
  - 80 um via diameter; 250um deep
  - Result: 0 failures (electrical and Optical) after 1000 Cy. TCB*

- Conformal Via Electrical Test Wafers (Backside TSV)
  - 200mm Wafers
  - 80 um via diameter, 200um deep
  - Result: 0 failures (no degradation in resistance) after 1000 Cy. TCB*

- Interposers and Capacitors
  - Si Interposers with TSV on top of Organic Substrate with diasy chain structures
  - 0/118 fails through 1000 Cy TCB*.
  - Capacitors: Test in progress. No failures through 250Cy TCB*.

Note (*) : Actual temperature delta during thermal cycling was 175C instead of 180C.
Capability Summary
Summary Capabilities

- **TSV:**
  - Via Dia 20um to 150um
  - Aspect Ratio: Up to 5  (up to 8 in development)
  - Front Side OR Backside
  - Wafer size: 150mm & 200mm (current). 300mm: In planning

- **Si Interposers with TSV and Capacitors**
  - Integrated Capacitors on Interposers
    - 1500 nF/cm2 with 3000nF/cm2 in development
  - Routing layers on either side
    - 2 um lines and spaces (90nm CMOS backend with partners 4-6F+ 1B 1yrs)
    - 5 um lines and spaces (Cu/PI 3F+1B 1yrs)
  - Test Device
    - I/Os
      - 4096 I/Os on top (65um dia, 125um pitch)
      - 1024 I/Os to BT (100um dia, 375um pitch)
  - Size: 12 mm x 12 mm;  TSV : 50 um dia, 300 um deep
  - Either Cu Pillar or Cu Pad; solder assembly to BT with underfill
Conclusions

- We have developed and applied Cu Filled TSV (Via First) and Conformal Cu TSV (Via Last) Technologies solving several key issues.
  - First order design and process interactions have been understood and integrated.
  - Excellent reliability results have been achieved after the key issues are resolved.
- Si Interposers for next generation advanced packaging have been developed.
  - Preliminary Reliability results are excellent passing 1000 cy TCB
  - High value decoupling capacitor technology is developed.
- Ready for scaling to production volumes
Thank you for your attention!

New Facility in Portland, OR
(60,000 Sq. ft. Clean Room in a 178,000 Sq. ft. facility.)