Greetings from the 3D Microsystems Packaging Research Center
IPC – June 14, 2010

ICs → 3D ICs → 3D Systems

Prof. Rao R. Tummala
Director, Packaging Research Center
Joseph M. Pettit Endowed Chair
Professor in ECE & MSE
Prof. Tummala’s Perspective

1. CMOs-based ICs face two challenges
   • Commodity
   • Reaching performance limits
2. 3D ICs viewed as potential solution; however,
3. 3D ICs face infrastructure, investment and cost issues
4. 3D ICs are Moore’s Law in 3D and only 20% of a system
5. Quantum jump in functionality can only come from 3D Systems as follow on 3D ICs
6. Packaging is therefore an enabler and an asset
7. Universities can play a major role in this new package-centric era
8. GT PRC is focusing on 3D Systems
GT PRC Vision (Prof. Tummala, 1993)

- SINGLE FUNCTION
- MULTI-FUNCTION
- MEGA-FUNCTION - Vision of GT PRC


W/S, PC, Laptop, Notebook, Cellular, SMART "Watch" 

Functional Density or Component Density / cm³
100-Function Watch(LG)

- The world’s very first, fully functioning 3G video conferencing phone into a size of a watch.
- Featuring:
  - full touch screen
  - built-in camera
  - built-in speaker
  - Bluetooth
- This bionic gadget can:
  - play music
  - take photos
  - work as a diary and a scheduler
  - read back your text messages
  - make video-calls
  - and much more.
- Let the Watchphone bring a serious sci-fi vibe into your life.
Home for SOP Concept
Integrated Approach to Research Education and Industry Collaboration

1. Leading Edge 3D Systems R&D
2. Educate Future Leaders
3. Collaborate with Global Industry & Academics
4. Enabled by $40M 300mm SOP Facility & Other Labs

- Demonstrated: SOP – RF, Digital, Optical
- Published: 1,150 Journal Papers
- Raised: $240M
- Graduated: 600 PhD & MS Students
- Collaborated: 150 Companies
- Cross-Discipline Faculty: 20
- Grad Students: 112
- New Faculty Produced: 9

Prof. Tummala, GT-PRC
Where do PRC Students Come?
And Where Do They Go?
Thanks for Great Contributions

James Meindl: Advisor

Madhavan Swaminathan: Electrical Design

CP Wong: Materials

Paul Kohl: Processes

Gary May: Manufacturing and Education

Joy Laskar: System Integration & RF

John Papapolymerou: RF SOP

Emmanouil Tentzeris: RF SOP

Thomas Gaylord: Opto SOP

GK Chang: Opto SOP

Mark Allen: Embedded Passives

Suresh Sitaraman: Mechanical Design

Prof. Tummala, GT-PRC
Packaging at GT Now is Campus-Wide
~$20-50 M/Yr

NRC
Meindl
HIGH FREQ.
Ralph
MIXED SIGNAL
Swaminathan
GEDC
Allen
THERMAL
Joshi
PRC
Tummala
NANO-MATL'S
Wong
IPC
Swaminathan
TEST
Chatterjee, Keezer
OPTICAL
Chang
RELIABILITY
Sitaraman
IFC
Kohl

2010

Prof. Tummala, GT-PRC
$150M Network of Advanced Packaging Labs @GT

$47M 3D Systems PRC

Prof. Rao Tummala

Reliability Modeling
Simulation

Prof. S. Sitaraman

Mixed Signal
Design & Test

Prof. Y. Joshi

Thermal
Measurement & Characterize

Prof. M. Swaminathan

Plating
Assembly

Prof. C. P. Wong

Substrate

Optical
Waveguides, Components Meas. & Char.

Prof. G.K. Chang

High Freq. Systems Lab
RF Meas. & Char.

Prof. S. Ralph

NRC / MiRC
S/C Processes MEMS, Sens.

Prof. J. Meindl

Prof. Tummala, GT-PRC

Prof. S. Ralph

11 | ICs to 3D ICs to 3D Systems
Grand Challenges in Microelectronics and Systems

- Electronics driven by ever-increasing performance or functionality at ever-reducing cost and size

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<th>Area</th>
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<th>Potential Solution</th>
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<td>Functionality</td>
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<td>Heterogeneous Modules</td>
<td>Glass and Si Packages</td>
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<td>Transistor Size</td>
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<td>Size of Wafer</td>
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<td>Miniaturized Systems</td>
<td>Limited by ICs, Packages &amp; Boards</td>
<td>3D ICs, Embedded ICs, SOP</td>
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Grand Challenges

- Technologies
- Investments and Profits
- Human Resources

What is the Role of Universities?
- Technologies
- Human Resources
- R&D and Manufacturing Infrastructure Investments – Not Manufacturing Investments
Role of PRC in Leading-Edge R&D

Exploratory Research
Strategic Research
Technology Development
Manufacturing

Technical Scope

GT PRC

Pre-competitive
- Govt. funded Research
- Research Consortia
- Infrastructure Network Consortia
- Contract Research

Industry

Competitive

Time in Years

10 5 2 0

14 | ICs to 3D ICs to 3D Systems
Prof. Tummala, GT-PRC
What is Packaging, Why and Trend?

What is Packaging?
- Interconnect, power, cool and protect ICs – Past
- Interconnect, power, cool and protect Systems – Future

Why Packaging?
- Device level:
  1. Must be packaged before KGD
  2. Sell as a discrete self-contained component; however
  3. Package cost is ~ IC cost
- System level: Interconnect to other components by SMT

Trend

- MCM 1985
- SIP 1995
- Embedded Actives & Passives 2010
SOC vs. MCM vs. 3D ICs

- **SOC**: 2 cm, 800 µm
- **MCM**: 2.25 cm, 2000 µm
- **3D ICs**: 500 µm
Grand Challenges in 3D ICs and Beyond

- Why do 3D ICs take so long from invention to product?
- When will it be a pervasive technology?
- Can university’s research have more impact?
- If so, how and under what conditions?
- Who will invest in new packaging technologies?
- What is PRC doing in these areas?
When Will 3D ICs Become Pervasive?

- Necessity
- Volume
- Cost
Can Universities Have More Impact?

Yes

- If University Programs Match Industry Needs

University Role

- Exploratory and Strategic R&D
- Well Educated and Globally-competitive Engineers
Who will Invest in the New Era?

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<th>Product Technology Hierarchy</th>
<th>Investment Hierarchy</th>
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<td>Package Companies</td>
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<td>Semiconductor Companies</td>
<td>System Integrators</td>
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<tr>
<td>Component Companies</td>
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<tr>
<td>Material &amp; Tool Companies</td>
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</table>
What is PRC Up To?
Industry-Centric PRC Model

Leading-edge & Fundamental Research

- Leading-edge R&D
- Globally-competitive Engineers
- Industry partnership

Cross-discipline & Industry-Centric Education

Global Industry Partnerships

Industry and Faculty Mentors

Cross-Discipline Projects and Teams

Industry & Academic Co-Ownership

Prof. Tummala, GT-PRC
U.S.-Fraunhofer Model at GT PRC

- Academic Faculty
- Graduate Students
- Industry Project Owner
- Research Faculty
Current Approach Creates Biggest Barrier to Systems:

- Lithographic Dimension (nm):
  - IC: 32nm
  - Package: 3,200nm
  - System: 100,000nm

- IC SYSTEM Gap ~ $10^5 \times$
- IC PACKAGE Gap ~ $10^4$
Georgia Tech-PRC Vision of 3D Systems

- 3D Systems
- 90% System
- 600mm SOP

GT PRC Focus
- 3D SYSTEMS
  - Consumer
  - Energy
  - Automotive
  - Healthcare
  - Computer

- Passive: R, L, C, Antennas
- Packages and Boards
- Thermal Materials and Interfaces
- Power Sources
- System Interconnections & Reliability
- System Design Tools

3D Systems

ICs to 3D ICs to 3D Systems

- 3D ICs- CMOS and non-CMOS
- 200- 300 mm wafers
- 10% System Miniaturization

Prof. Tummala, GT-PRC
SOC vs. 3D ICs vs. SOP

Best of IC Integration by SOC

- Highest functionality
- Smallest size
- Lowest cost

MOORE'S LAW DRIVE

SYSTEM'S LAW DRIVE

Best of Package Integration by 3D ICs < SIP < MCM

Best of System Integration by SOP < SOPOB
GT-PRC’s Vision

NANOMATERIALS

EMBEDDED COMPONENTS

INTERCONNECTIONS

SUBSTRATES & SYSTEM INTEGRATION

OPTO SOP

DIGITAL SOP

ANALOG & RF SOP

SENSORS

THERMAL SOP

EBG & Isolation

Antennas & Filters

MEMS PACKAGING

Silicon, Glass, or Organic Core with TPV

3D CAPACITORS

3D ICs

MECHANICAL DESIGN FOR RELIABILITY

HIGH DENSITY I/O

MIXED SIGNAL ELECTRICAL DESIGN

THERMAL

POWER & BATTERIES

3D CAPACITORS

NANOMAGNETICS

Bio-Sensor

MEMS PACKAGING

Prof. Tummala, GT-PRC
Single Technology Platform for Systems-3D ASSM

Moore's Law

3D All Silicon System

Component Density or Functional Density/cm³

Transistors/cm³


MCM PTH SMT SOP

MICRO NANO

ICs and 3D ICs

Systems

Sources: IBM, Intel

Prof. Tummala, GT-PRC
Seven PRC Core Teams

1. Electrical Design
   Prof. Swaminathan (ECE)
   Prof. S. K. Lim (ECE)

2. Mechanical Design
   Prof. S. Sitaraman (ME)
   Dr. R. Pucha (ME)

3. Nano Materials
   Prof. C. P. Wong (MSE)
   Dr. H. Sharma (MSE)

4. Thermal Technology
   Prof. Y. Joshi (ME)
   Dr. Y. J. Kim (ME)

5. Nano-scale Components
   Prof. R. Tummala (MSE)
   Dr. P. M. Raj (ECE)

6. Interconnections, Assembly & Reliability
   Prof. R. Tummala (MSE)
   Mr. N. Kumbhat

7. Systems Integration
   Prof. R. Tummala (MSE)
   Dr. V. Sundaram (ECE/MSE)
### WLP vs. Panel-based Si/Glass Package

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>WLP</th>
<th>Interposer</th>
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<tbody>
<tr>
<td>Large Wafer or Panel</td>
<td>✅</td>
<td>✅</td>
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<tr>
<td>Miniaturized Components</td>
<td>✅</td>
<td>✅</td>
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<tr>
<td>Low-cost Materials and Processes</td>
<td>✅</td>
<td>✅</td>
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<tr>
<td>High-throughout Tools</td>
<td>✅</td>
<td>✅</td>
</tr>
<tr>
<td>Low-cost Facilities</td>
<td>✅</td>
<td>✅</td>
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<tr>
<td>Smallest Package Size</td>
<td>✅</td>
<td>✅</td>
</tr>
<tr>
<td>Thermal Performance</td>
<td>✅</td>
<td>✅</td>
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</tbody>
</table>

- **Wafer-based Si Interposer or WLP**
  - 200-300 mm Wafer

- **Panel-based Glass or Si Package**
  - 600 mm System-On-Panel

8X

---

Prof. Tummala, GT-PRC
Why Glass?

- **Two Reasons**
  - Potential for 10 X Lower cost than Si
  - Best Electrical Resistivity

- **Two Shortcomings**
  - Low cost Via
  - Lower Thermal Conductivity than Si but better than organic packages
### Ideal Properties of a Package Material

<table>
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<tr>
<th>Characteristic</th>
<th>Ideal Properties</th>
<th>Materials</th>
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<tr>
<td></td>
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<td>Glass</td>
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<tr>
<td><strong>Electrical</strong></td>
<td>• High resistivity</td>
<td>Good</td>
</tr>
<tr>
<td></td>
<td>• Low loss</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Physical</strong></td>
<td>• Smooth surface finish</td>
<td>Good</td>
</tr>
<tr>
<td></td>
<td>• Large area availability</td>
<td>Good</td>
</tr>
<tr>
<td></td>
<td>• Ultra thin</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td>• High Conductivity</td>
<td>Good</td>
</tr>
<tr>
<td></td>
<td>• CTE matched to Si</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Mechanical</strong></td>
<td>• High strength</td>
<td>Good</td>
</tr>
<tr>
<td></td>
<td>• High modulus</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Chemical</strong></td>
<td>• Resistance to process chemicals</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Processability</strong></td>
<td>• Ease of Via formation and metallization</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>• Low cost per I/O at 25um pitch</td>
<td>Good</td>
</tr>
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</table>
Why Panel-based Glass & Si Packages?

Panel-Based Glass & Si Packages

Cost/I/O Pitch (um)

10x

1x

3D ICs

2D ICs

I/O Pitch (um)

50 100 150 225

Wafer-Based Silicon Interposer

Ceramic

Organic

Panel-Based Glass & Si Packages

Prof. Tummala, GT-PRC

ICs to 3D ICs to 3D Systems
### 1st Demonstration of Glass Package @50 µm Pitch

#### TPV fill 50µm pitch vias
- Via entrance: 35 µm
- Via exit: 22 µm
- TPV pitch: 50 µm
- Glass thickness: 175 µm

#### TPV fill 250µm pitch vias
- Via entrance: 150 µm
- Via exit: 50 µm
- TPV pitch: 250 µm
- Glass thickness: 175 µm

---

4 Metal layer on glass
Superiority of Glass over Si

EM Model

Si
Glass
TPV
100 µm
100 µm
30 µm

Polymer or SiO$_2$ Liner

Superiority of Glass over Si

S21 (dB)

Si 10ohm-cm, 5 µm polymer liner
Si 10ohm-cm, 0.1 µm SiO$_2$ liner
Interconnections
IC Package Interconnection Trend

- Wire Bond
- Flip Chip
- TSV & Interconn.
- Chip- First
- Chip- Last

Prof. Tummala, GT-PRC
Chip 1st vs. GT’s Chip-Last

1A. Embedded Die
(Imbera)

1B. Fan-out Wafer Level Packaging
(Infineon, ST Micro, Stats Chip Pack, ASE)

2. Chip-Last: Ultra-thin 3D Embedded Actives and Passives (EMAP)
(Georgia Tech)
Why Chip-last Embedding

- Wirebond
- Flip-Chip
- Chip-First
- Chip-Last

- New Infrastructure
- Testability
- Repairability
- New Business Model

I/O Density (per Chip area)

Yield and Manufacturability

1x ~4x ~40x ~40x
Chip-Last Embedded ICs with Chip-First Benefits

- Demonstrated 55µm Thick IC Embedding in 6-layer Substrate
- Total package profile with 2 stacked ICs ~ 0.25mm
- 50µm pitch Cu interconnects (15µm total height) to substrate
- Completed 1000 Thermal Shock Cycles without failure
Chip-Last Reliability: ~550µm Die on Surface

3mm

25mm

Die Thickness ~ 550µm

TST DATA > 2200 cycles

PART OF WORKING DAISY CHAIN AFTER 2000 CYCLES
Industry Collaboration Vision

- Partnership with Global Industry for:
  - Leading-edge R&D
  - IP Development
  - Manufacturing Infrastructure
  - Facilities Usage
  - Human Resources
  - Industry Education
  - Advise and Consult
7 Reasons to Collaborate with GT-PRC

1. R&D beyond the current focus of your company
2. Alternative technology options to your own
3. Lower cost than in-house R&D
4. Industry-wide manufacturing infrastructure development
5. Friendly access to new Intellectual Property
6. PRC team, expertise and R&D facilities at GT to demonstrate the new technology
7. Well-educated engineers in tomorrow’s technology for recruitment
15 Years of Technology Transfer Legacy in Ultra-miniaturized Systems

- Technology Transfer
  - 249 Inventions Recorded (Know How and Patented)
  - 80 Patents Filed, 36 Patents Issued, 6 Pending
  - 39 Royalty-bearing Licenses + 127 Non-Royalty Bearing Membership
  - 97 Specifically Identified Tech Transfer Examples to:
    - Siemens, Raytheon, Samsung Electronics, Samsung Techwin, Ericsson, AMD, DuPont, IBM, Motorola, Lambda, Triquint Semiconductor, National Semiconductor, HP/Agilent, Medtronic, Delco, Cadence, Sun Microsystems, BF Goodrich, Siemens, Boeing, GE, National Starch, Rogers, Sandia, Qualcomm, Intarsia, Texas Instruments, Intel, Nitronex, Cypress Semiconductor, Promerus, Harima Chemicals, Rambus, Rohm & Haas, and more
Education Challenge
Educational Vision

- Goal: “Interdisciplinary Individual”

**Electrical Sciences**
- Low impedance power feed
- Low inductance/high capacitance
- Cross talk
- Attenuation

**Mechanical Sciences**
- Efficient and cost effective thermal transfer
- Interfacial stresses
- Fatigue
- Warpage
- Creep

**Material Sciences**
- Dielectrics
- Conductors
- C,L,R,Antennas
- Multilayer structures

**Chemical Sciences**
- Lithographic processes
- Microstructure development
PRC's Text and Reference Books & 26 Courses

First Undergraduate Textbook

First Graduate Textbook

Packaging Materials

Power Integrity Modeling
# Packaging Courses @GT

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<th>Course</th>
<th>Title</th>
<th>ECE</th>
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Summary

1. Packaging:
   • Past – A Necessary Evil,
   • Now – An Asset

2. If We Can Make 1 Billion Transistor Chip,
   We Can Make Mega-functional Systems

3. An SRC Workshop that Brings Together Industry & Academics in IC and Package is Very Critical
Thank You

Prof. Rao R. Tummala
Director, Packaging Research Center
Joseph M. Pettit Endowed Chair
Professor in ECE & MSE