Stress Analyses and Mechanical Reliability of 3D Interconnects with Through-Silicon Vias

Kuan (Gary) Lu\textsuperscript{1}, Suk-Kyu Ryu\textsuperscript{2}, Xuefeng Zhang\textsuperscript{1}, Jay Im\textsuperscript{1}, Paul S. Ho\textsuperscript{1}, Rui Huang\textsuperscript{2}

\textsuperscript{1}Microelectronics Research Center
\textsuperscript{2}Department of Aerospace Engineering and Engineering Mechanics
University of Texas at Austin

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Wafer Level 3D Integration

Mechanical effects:
- Through silicon vias (TSVs)
- Wafer thinning
- Wafer (die) bonding

Philip Garrou, Microelectronic Consultants of NC

Memory stacks (Samsung)

Intel 300 mm multicore processors
**Through Silicon Vias**

**Via first processes**

**TSV materials:**
- Conductors: Cu, W
- Insulators: TEOS, polymers
- Barrier/adhesion: TiN, TaN

**Geometric aspects:**
- High aspect ratio
- Thin Si wafer (~10-300 µm)
- Diameter (~1-50 µm)
- Pitch (~3-100 µm)

Bower et al. (RTI), ECTC 2006
Eric Beyne (IMEC), IITC 2006
TSV Mechanical Reliability

➢ **Stresses around TSVs:**
  - Cracking of silicon
  - Strain-induced mobility changes in transistors (piezoresistance effect)
  - *Keep-away zone* for FEOL

➢ **Stresses inside TSVs:**
  - Plastic deformation
  - Stress-induced voiding
  - Stress migration

➢ **Stresses at the interfaces:**
  - Debonding, via pop-up

❖ **Possible origins of stresses:**
  - Thermal expansion mismatch between Si and via materials
  - Packaging induced deformation (warping)
  - Electromigration
Thermal Stress: Method of Superposition

- For a high aspect-ratio TSV, the stress field away from the surfaces can be obtained from a 2D plane-strain solution (Problem A).

- The stress field near surface is 3D, which can be determined by superimposing an opposite surface loading (Problem B) onto the 2D field (Problem A) to satisfy the boundary conditions at the surface.
2D Plane-Strain Solution (Problem A)

Thermal Strain:

\[ \varepsilon_T = -(\alpha_{Cu} - \alpha_{Si})\Delta T \]

Uniform thermal stress in Cu via (triaxial):

\[ \sigma_r = \sigma_\theta = \frac{E\varepsilon_T}{2(1-\nu)}, \quad \sigma_z = \frac{E\varepsilon_T}{1-\nu} \]

Stress distribution in Si (biaxial):

\[ \sigma_r = -\sigma_\theta = \frac{E\varepsilon_T}{2(1-\nu)} \frac{a^2}{r^2}, \quad \sigma_z = 0 \]

- The magnitude of the stresses in the via is independent of the via size.
- The stresses in Si decay with the distance \((r)\), with the decay length proportional to the via size \((a)\).
Effect of elastic mismatch

\[ \sigma_r \propto \frac{a^2}{r^2} \]

\[ \sigma_\theta \propto -\frac{a^2}{r^2} \]

<table>
<thead>
<tr>
<th></th>
<th>Elastic Modulus (GPa)</th>
<th>CTE (ppm/C)</th>
</tr>
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<tbody>
<tr>
<td>Si</td>
<td>130.2</td>
<td>2.3</td>
</tr>
<tr>
<td>Cu</td>
<td>104.2</td>
<td>17.0</td>
</tr>
</tbody>
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\[ \Delta T = -380 \, ^\circ C \]
Effect of liner layer

A soft liner layer between the Cu via and Si dramatically reduces the stresses in both the via and Si.

$\Delta T = -380 \, ^\circ C$

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<tr>
<td>SiCOH</td>
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</tr>
<tr>
<td>Cu</td>
<td>104.2</td>
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</tr>
</tbody>
</table>
2D Stress Field of Single Via

- Assume stress free at high temperature (reference)
- Cooling from the reference temperature ($\Delta T = -175^\circ$C) leads to tensile stresses in the via.
- Around the via, the stress is tensile in the radial direction and compressive in the circumferential direction, both concentrated near the via.
Stress Interaction between Two Vias ($\sigma_x$)

- Elastic interaction between TSVs depends on the via size and pitch
- Distribution of specific stress component depends on the relative arrangement of the vias.

(TSV diameter: 20 um)
Assume devices sensitive to normal stress $\sigma_x$.

The keep-away zone can be optimized by properly arranging the TSVs with the same via density.
3D Stress Analyses of TSVs

- **Analytical solution**
  - Near-surface stress distribution by the method of superposition

- **Finite element analysis**
  - Effect of wafer thickness
  - Effect of liner interlayer
3D Stress Field near Surface (Problem B)

Uniform surface pressure over a circular area

\[ p = \sigma_z^T = \frac{E\varepsilon_T}{1 - \nu} \]

- Stress decays with the distance from the surface.
- Triaxial stress in the via center \((r = 0)\).
- Radial and circumferential stresses on the surface \((z = 0)\).
- Shear stress at the interface.

\[ \sigma_z(r = 0) = \frac{E\varepsilon_T}{1 - \nu} \left[ \frac{z^3}{(a^2 + z^2)^{3/2}} - 1 \right] = \frac{E\varepsilon_T}{1 - \nu} f \left( \frac{z}{a} \right) \]

\[ \sigma_r(r = 0) = \sigma_\theta(r = 0) = \frac{E\varepsilon_T}{2(1 - \nu)} \left[ -2\nu + \frac{(1 + 2\nu)z}{\sqrt{a^2 + z^2}} + \frac{a^2z}{(a^2 + z^2)^{3/2}} \right] \]
\[
\sigma_z(r, z) = -\int_0^{2\pi} \int_0^a \frac{3pz^3 \rho d\rho d\theta}{2\pi \left(\rho^2 + r^2 - 2\rho r \cos \theta + z^2\right)^{5/2}}
\]

\[
\sigma_{zr}(r, z) = -\int_0^{2\pi} \int_0^a \frac{3pz^2 (r - \rho \cos \theta) \rho d\rho d\theta}{2\pi \left(\rho^2 + r^2 - 2\rho r \cos \theta + z^2\right)^{5/2}}
\]
3D Stress Fields near Wafer Surface

\[
\sigma_r = \frac{p}{2\pi} \int_0^a \int_0^{2\pi} \left[ \frac{1 - 2\nu}{r^2 + z^2 + z\sqrt{r^2 + z^2}} - \frac{3zr^2}{(r^2 + z^2)^{5/2}} \right] \cos^2 \beta + \left\{ \frac{(1 - 2\nu)z}{(r^2 + z^2)^{3/2}} - \frac{1 - 2\nu}{r^2 + z^2 + z\sqrt{r^2 + z^2}} \right\} \sin^2 \beta \right] \rho \, d\rho \, d\theta
\]

\[
\sigma_\theta = \frac{p}{2\pi} \int_0^a \int_0^{2\pi} \left[ \frac{1 - 2\nu}{r^2 + z^2 + z\sqrt{r^2 + z^2}} - \frac{3zr^2}{(r^2 + z^2)^{5/2}} \right] \sin^2 \beta + \left\{ \frac{(1 - 2\nu)z}{(r^2 + z^2)^{3/2}} - \frac{1 - 2\nu}{r^2 + z^2 + z\sqrt{r^2 + z^2}} \right\} \cos^2 \beta \right] \rho \, d\rho \, d\theta
\]
Comparisons between 3D and 2D solutions
Effect of Wafer Thickness

$\sigma_z$

$H/D=2$

$H/D=10$

$\sigma_{rz}$

$\sigma_r$
Effect of Wafer Thickness

Stresses at the center of TSV:

- The stresses in the TSV decrease as the aspect ratio $H/D$ decreases.

$$
\text{Normalized Stress} \left( \frac{\sigma_z}{p} \right)
$$

$z/H$ vs $\frac{\sigma_z}{p}$ for different aspect ratios $H/D$.
Stresses acting at the via/Si interface:

- The opening stress ($\sigma_r$) at the interface decreases as the aspect ratio H/D decreases.
- The shear stress ($\sigma_{rz}$) at the interface increases as the aspect ratio H/D decreases.
Effect of Liner Interlayer

\[ \sigma_r \]

\[ \sigma_\theta \]

Without liner  
With liner
Effect of Liner Interlayer

\(\sigma_z\)

\(\sigma_{rz}\)

Without liner

With liner
R-crack grows in Si when the circumferential stress is tensile ($\sigma_\theta > 0$, $\Delta T > 0$).

C-crack grows in Si when the radial stress is tensile ($\sigma_r > 0$, $\Delta T < 0$).

Interfacial crack grows under mixed mode with the normal stress $\sigma_r > 0$ ($\Delta T < 0$) and shear stress $\sigma_{rz}$ ($\Delta T > 0$ or $\Delta T < 0$).
TSV-induced R-crack in Si

Stress intensity factor:

\[ K_I(c) = \frac{E\Delta\alpha\Delta T}{1-\nu} \sqrt{\frac{\pi c}{8(1+c/a)^3}} \]

Energy release rate:

\[ G(c) = \frac{K_I^2}{E} = \frac{\pi E(\Delta\alpha\Delta T)^2}{8(1-\nu)^2} \frac{c}{(1+c/a)^3} \]

- The energy release rate for a R-crack increases as the via diameter increases.

- The maximum energy release rate occurs at the crack length \( c = 0.5a \):

\[ G_{\text{max}}(a) = \frac{\pi(\Delta\alpha\Delta T)^2}{54(1-\nu)^2} Ea \]
Summary

- Analysis of thermal stresses in and around TSVs
  - 2D analysis: interactions of TSV arrays
  - 3D analysis: near-surface field
  - FEA models: effects of wafer thickness and liner interlayer

- Fracture modes of TSVs
  - R-crack in Si: energy release rate increases with via diameter.
  - C-crack in Si: study in progress
  - Interfacial crack: study in progress

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